Synopsis V1.0
SEE Test Report for the Samsung and Elpida DDR2 SDRAM

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Test Date: 3/28-3/29/07(IUCF), 6/24-6/27/07(TAMU), 8/11-14/07(TAMU)
Report Date: 9/21/07

I. Introduction

This study was undertaken to determine the susceptibility of the Samsung K4T1G044QA-ZCD5 and Elpida EDE1104AB-50-E Gbit DDR2 DRAM to destructive and nondestructive single-event effects (SEE) due to protons and heavy ions. The devices were monitored for SEUs, functional interrupts and destructive events induced by exposing it to a 198 MeV proton beam at the University of Indiana Cyclotron Facility (IUCF) and to heavy ions at the Texas A&M University (TAMU) Cyclotron Institute.

II. Devices Tested

We tested 2 die of each part marked with date codes 0625 CWD089A1 (Samsung) and 06310WCFW (Elpida). Note that with commercial devices, the same lot date code is no guarantee that the devices are from the same wafer diffusion lot or even from the same fabrication facility. However, we believe that since these devices are fabricated in the still relatively rare 90 nm feature-size technology and were supplied by the manufacturer that their provenance is traceable.

Both devices are 90-nm-minimum-feature-size CMOS Double-Data-Rate Synchronous Dynamic Random Access Memory.

III. Test Facility

Facilities: IUCF, TAMU

Flux: (5×10^5 to $1. \times 10^9$ protons/cm^2/s @IUCF); (5×10^2 to $1. \times 10^5$ ions/cm^2/s @TAMU).

Fluence: Proton fluences at IUCF varied due to the needs of the IUCF for therapies. However, most irradiations were conducted to a fluence of 8.37×10^{10} particles/cm^2 unless they were interrupted. Most irradiations at TAMU ended with a device losing functionality due to a single-event functional interrupt after ~1×10^4 ions per cm^2.

Table I: Ions/Energies and LET for this test

Ion	Energy/AMU	Angle	Facility	Incident LET (active vol.)	Residual Range (normal)
Proton	198, 89	Various	IUCF	N/A	Not a factor
Ne	25	0°,60°	TAMU	~2	>600
Ar	25	0°,30°,45°60°	TAMU	~7.	>350
Kr	25	0°,60°,	TAMU	~22	>200
Xe	25	0°,60°	TAMU	~54	>100

Test Conditions

Test Temperature: Room Temperature
Operating Frequency: 200 MHz external clock.
Power Supply Voltage: 1.8 V.

IV. Test Methods

Because of the mode of operation of DRAM, all testing was performed dynamically at an external clock speed of 200 MHz (DDR speed of 400 MHz) and with a test pattern of (55AA).

The Block diagram for control of the DUT is shown in Figure 1. The FPGA based controller interfaces to the FLASH daughter card and to a laptop, allowing control of the FPGA and uploading of new FPGA configurations and instructions for control of the DUT. Power for the DUT is supplied by means of a computer-controlled power supply. The National Instruments Labview interface monitors the power supply for overcurrent conditions and shuts down power to the DUT if such conditions are detected.

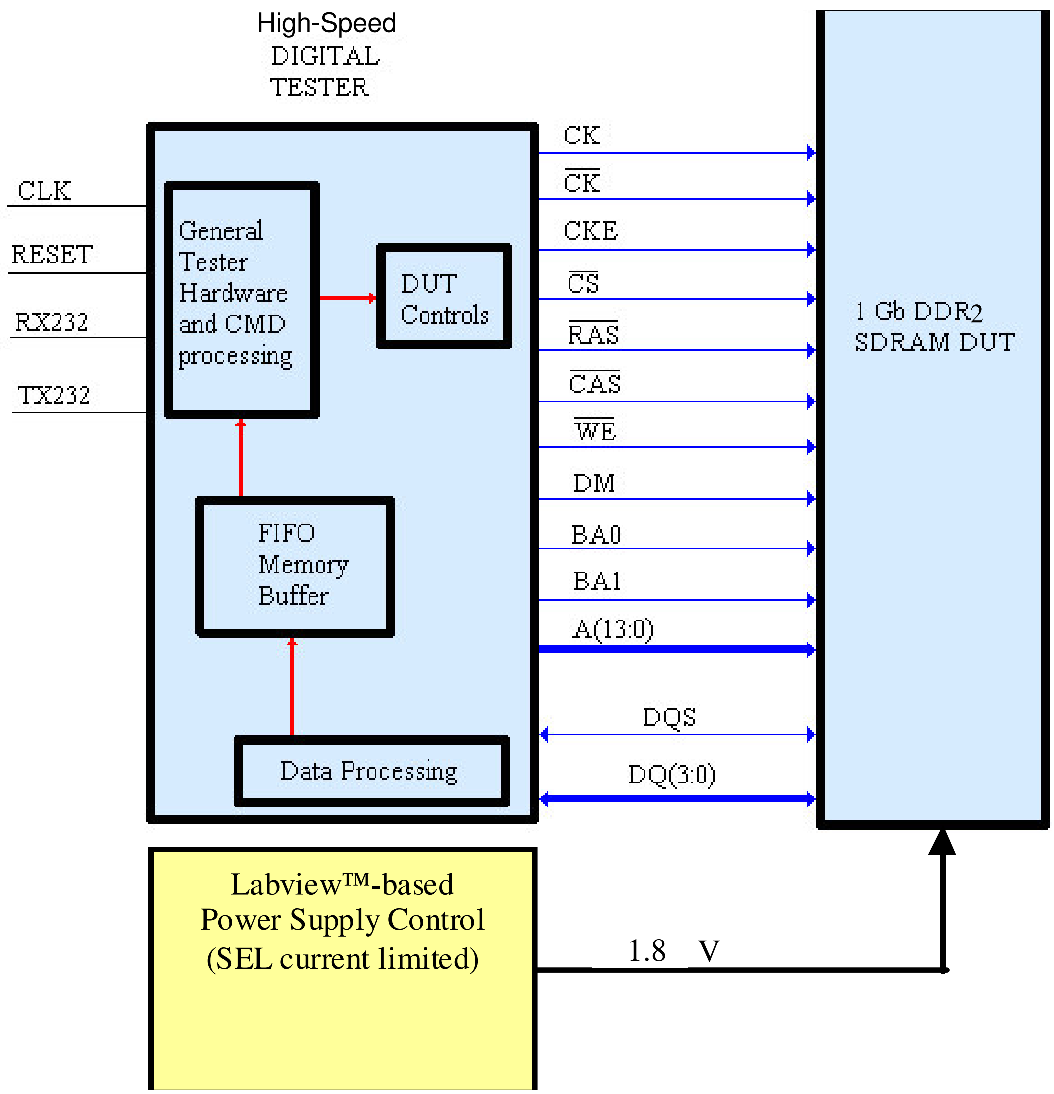

Figure 1. Overall Block Diagram for the testing SDRAMs with the High-speed tester.

V. Proton Results

During testing at IUCF, the memories were irradiated with 198 and 89 MeV protons both at normal incidence and at 60° to the normal (the maximum angle possible without exposing the tester to the proton flux. Moreover, tilting of the DUT was possible only about the vertical axis for the same reason. No SEL or other high-current events were seen during proton irradiation of these devices. Single-bit SEU (within a data word) and SEFI were observed for both devices. However, the cross section for SEU for the Elpida device may be contaminated by SEFI at the higher proton energy. Based on testing of past past Elpida memories and discussions with Paul Rutt of Seakr, it is thought that most of these SEFI could be fixed by refreshing mode registers. However, this was not possible given the test software and hardware configuration available for this test. Figure 1 shows the cross sections for SEU and SEFI for the Samsung and Elpida memories (averaged over devices, since no significant part-to-part variation was seen). Data are presented by vendor (labeled S or E) and by proton incident angle (0 or 60°) as a function of proton energy. No clear trend is evident for angle of incidence, and proton cross sections for the Samsung device increased only slightly with energy, indicating a much lower proton energy threshold.

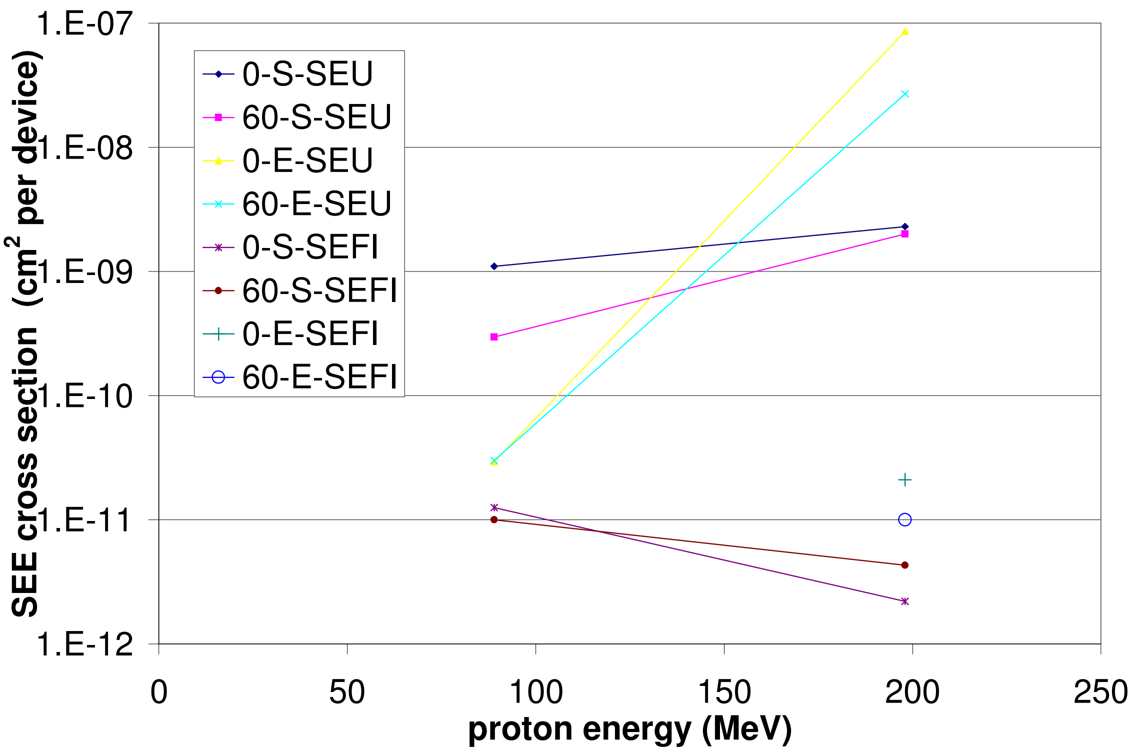

Figure 2 Proton SEU and SEFI cross sections for Samsung (S) and Elpida (E) as a function of proton energy and for normal and 60° off normal incidence.

No obvious incidence of stuck bits was seen either during the run or during post processing.

No significant asymmetry between bit flips 1 to 0 was seen versus 0 to 1. During proton testing, the devices received roughly 100 krad(Si) and showed little evidence of degradation.

VI. Heavy Ion Results

Processing of heavy-ion data was complicated by the occurrence of many different types of SEFI. Because the state machine of the device cannot be reliably identified after the occurrence of a SEFI, we estimated SEU rates only with upsets that occurred before the onset of the first block error/SEFI, even if the device seemed to recover after a short time. Likewise, even if there was evidence of multiple independent SEFI, we only consider the first SEFI per run. The cross sections were determined using fluence values estimated from the flux during the run and the time at which the first SEFI occurred.

LET values were estimated by starting with the nominal ion LET and energy and transporting the ion through the 100 micron overburden on top of the device active volume (weighted by the secant of the angle of incidence).

SEU were seen down to the lowest test LET (~1.8 MeVcm^2/mg). Onset of SEFI was seen at about 4 MeVcm^2/mg for the Samsung and about 6 MeVcm^2/mg for the Elpida. The Elpida device was susceptible to SEL at elevated temperature (~80 °C) with an onset LET somewhere between 14 and 50 MeVcm^2/mg, while no SEL was seen for the Samsung device for elevated temperature and LET>100 MeVcm^2/mg.

Significant deviations from the expected 1/cosθ effective LET dependence were seen for the Samsung SEU cross section vs. LET curve—especially at low LET. Such behavior was not seen for the Elpida device, nor for the SEFI behavior of the Samsung device.

Multibit upsets were seen for the Samsung device starting at an LET of about 23 MeVcm^2/mg. No MBUs were seen for the Elpida devices, but this may be because of the much more limited statistics for these devices.

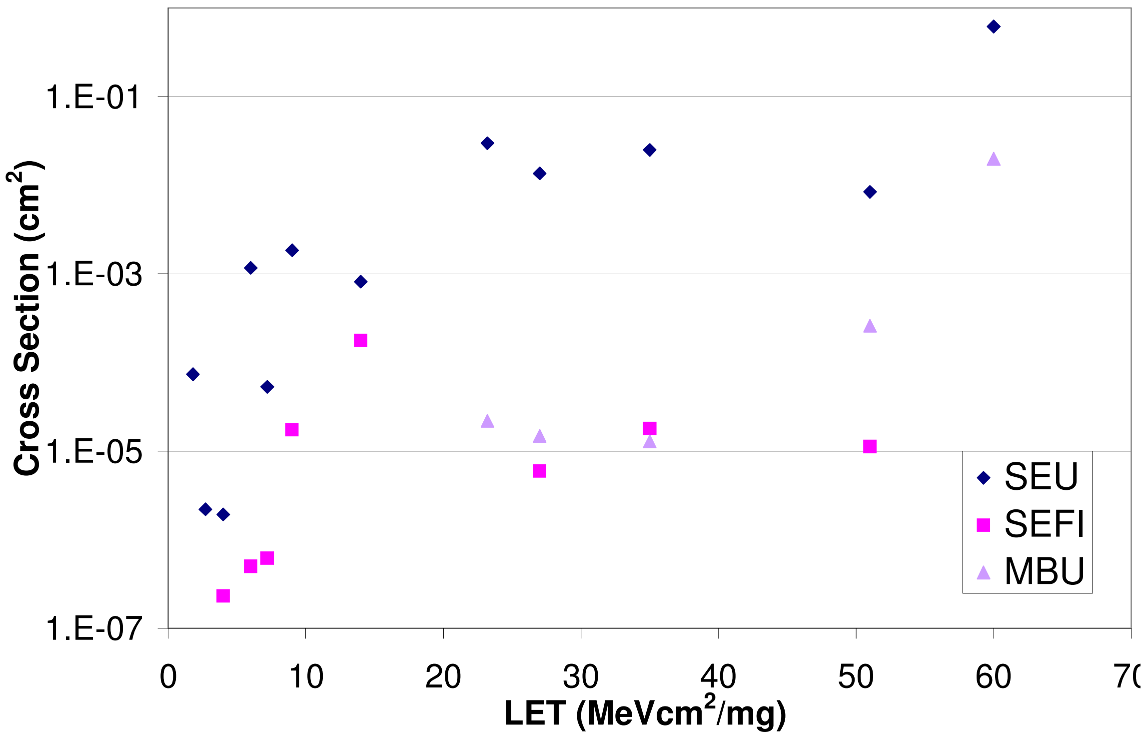

Figure 3 SEU, MBU and SEFI cross section vs. LET curves for Samsung DDR2 devices.

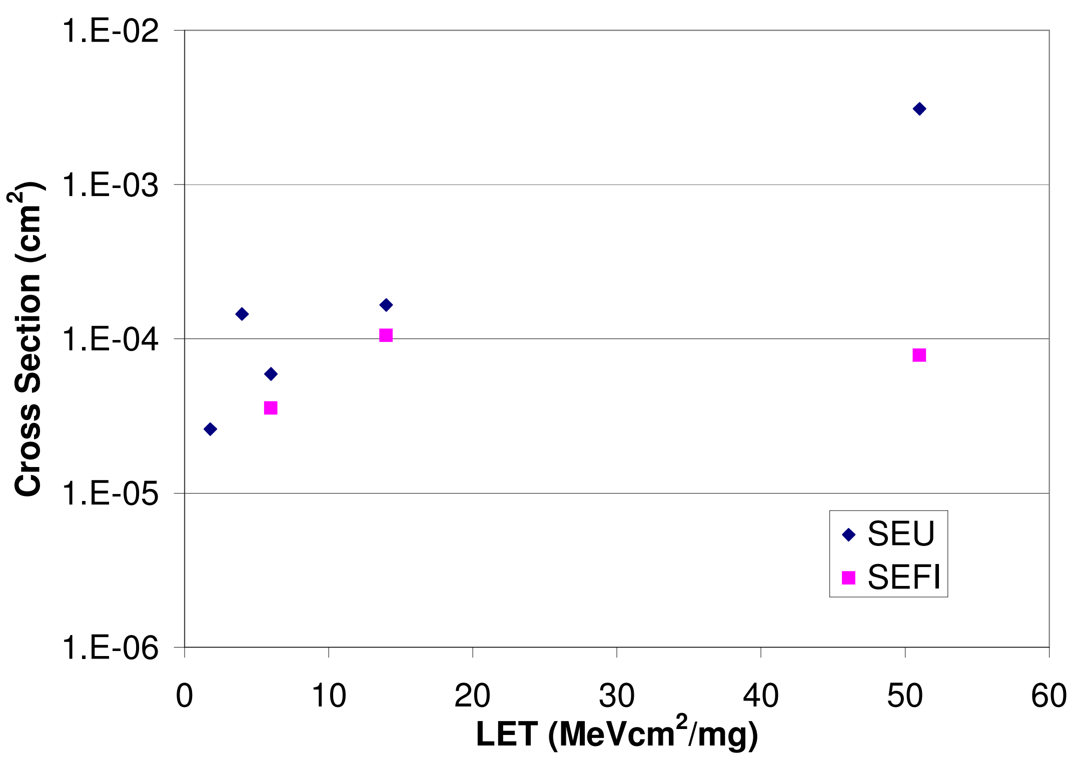

Figure 4 SEU, MBU and SEFI cross section vs. LET curves for Elpida DDR2 devices.

VII. Further Test Requirements

This test represents a preliminary characterization of SEE vulnerability of the Samsung K4T1G044QA-ZCD5 and Elpida EDE1104AB-50-E Gbit DDR2 DRAMs. Additional heavy ion testing is required before these devices can be considered for space applications. Such testing would involve a better determination of the onset LET for SEL, SEU, MBU and SEFI. While the SEL mode observed did not destroy the part (we did have current limiting), additional testing to ensure all SEL modes are nondestructive and do not result in latent damage is highly desirable. Additional TID testing will be carried out to determine sensitivity to this degradation mode.